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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	09/849734
				Filing Date	05/04/01
				First Named Inventor	G. Glenn Henry Thomas C. McDonald
				Group Art Unit	2183
				Examiner Name	Henry W. H. Tsai
Sheet	1	of	2	Attorney Docket Number	CNTR.2023

U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup>			
HA	AA	5142634		Fite et al	08/25/1992	
	AB	5163140		Stiles et al	11/10/1992	
	AC	5353421		Emma et al	10/04/1994	
	AD	5355459		Matsuo et al	10/11/1994	
	AE	5404467		Saba et al	04/04/1995	
	AF	5530825		Black et al	06/25/1996	
	AG	5850543		Shiell et al	12/15/1998	
	AH	5867701		Brown et al	02/02/1999	
	AI	5948100		Hsu et al	09/07/1999	
	AJ	5964868		Gochman et al	10/12/1999	
	AK	5974543		Hilgendorf et al	10/26/1999	
	AL	5978909		Oded Lempel	11/02/1999	
	AM	6044459		Bae et al	03/28/2000	
	AN	6108773		Col et al	08/22/2000	
	AO	6151671		D'Sa et al	11/21/2000	
	AP	6314514		Thomas C. McDonald	11/6/2001	
	AQ	6601161		Rappoport et al	07/29/2003	
	AR	6647467		Eric M. Dowling	11/11/2003	

Examiner Signature	<i>Henry W. H. Tsai</i>	Date Considered	2/1/05
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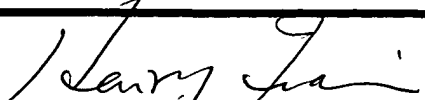
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Sheet	2	of	2	Attorney Docket Number	CNTR.2023

OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
215	BA	SAKAMOTO ET AL; <u>Microarchitecture Support for Reducing Branch Penalty in a Superscaler Processor</u> ; pp. 208-216; IEEE 1996; Mitsubishi Electric Corp., System LSI Laboratory, 4-1 Mizuhara, Itami, Hyogo 664, Japan.	
	BB	YEH ET AL; <u>ALTERNATIVE IMPLEMENTATION OF TWO-LEVEL ADAPTIVE BRANCH PREDICTION</u> ; 19 <sup>TH</sup> Annual International Symposium on Computer Architecture, pp. 124-134, May 19-21, 1992, Gold Coast, Australia.	
	BC	CHANG ET AL; <u>ALTERNATIVE IMPLEMENTATIONS OF HYBRID BRANCH PREDICTORS</u> ; Proceedings of MICRO-28, 1995, IEEE.	
	BD	MC FARLING, SCOTT; <u>WRL TECHNICAL NOTE TN-36</u> , "Combining Branch Predictors, June 1993, Western Research Laboratory, 250 University Ave., Palo Alto, CA 94301	
	BE	IEEE 100; <u>THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS</u> ; Seventh Edition, IEEE, Standards Information Network, IEEE Press,	
	BF	BRAY ET AL; <u>STRATEGIES FOR BRANCH TARGET BUFFERS</u> ; Technical Report No. CSL-TR-91-480, June 1991.	

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